What is claimed is:

1. A MOSFET structure comprising:

a semiconductor substrate having pedestals integrally formed on a surface of the semiconductor substrate, the pedestals having a top portion and a stem portion;

a gate insulator layer superjacent the top portion of the pedestal; and

a gate electrode overlying the gate insulator layer.

2. The MOSFET structure of Claim 1, wherein the top portion of the pedestal has impurity doped source and drain portions.

3. The MOSFET structure of Claim 1, wherein the top portion of the pedestal includes spacers at the distal ends.

4. The MOSFET structure of Claim 1, wherein a volume defined, at least in part, by the stem and top portion of a pedestal is substantially filled with a dielectric material.

5. The MOSFET structure of Claim 1, wherein a volume, defined at least in part by the stem and top portion of the pedestal, is substantially filled with at least two dielectric materials.

6. The MOSFET structure of Claim 5, wherein one of the at least two dielectric materials is an oxide of silicon.

7. The MOSFET structure of Claim 5, wherein one of the at least two dielectric materials is a gas.

8. The MOSFET structure of Claim 7, wherein the gas is air.

9. The MOSFET structure of Claim 5, wherein one of the at least two dielectric materials is undoped polysilicon.

10. The MOSFET structure of Claim 5, wherein one of the at least two dielectric materials is a polymer.

11. The MOSFET structure of Claim 10, the polymer has a dielectric constant that is less than the dielectric constant of silicon dioxide.

12. The MOSFET structure of Claim 1, further comprising an oxide liner on both the stem portion of the pedestal, and the underside of the top portion of the pedestal.

13. The MOSFET structure of Claim 12, wherein a volume defined, at least in part, by the oxide-lined stem and oxide-lined top portion of the pedestal is substantially filled with a dielectric material.

14. The MOSFET structure of Claim 12, wherein a volume defined, at least in part, by the oxide-lined stem and oxide-lined top portion of the pedestal is substantially filled with at least two dielectric materials.

15. A method of forming an isolated junction field effect transistor comprising:

a) depositing a layer of trench masking material on a surface of a semiconductor substrate;

b) patterning the layer of trench masking material to expose portions of the semiconductor substrate;

c) etching the semiconductor substrate to form at least one trench, wherein each of the at least one trenches has a bottom surface and a side surface;

d) depositing a conformal layer of spacer material;

e) forming spacers adjacent to the trench side surfaces by anisotropically etching the spacer material until the semiconductor substrate at the bottom surface of the at least one trench is exposed;

f) isotropically etching the exposed semiconductor substrate;

g) filling each of the at least one trenches with at least one dielectric material;

h) forming a gate insulator layer;

i) forming a gate electrode over the gate insulator layer; and

j) implanting impurities to form a source and a drain region.

16. The method of Claim 15, wherein the depth of the trench is substantially equal to a predetermined junction depth.

17. The method of Claim 15, wherein the depth of the trench is greater than a predetermined junction depth.

18. The method of Claim 15, wherein the spacer layer material is a material selected from the group consisting of silicon oxide and silicon nitride.

19. The method of Claim 15, wherein filling each of the at least one trenches with at least one dielectric material comprises partially filling the undercut portions of the trenches with an oxide of silicon such that an air gap exists adjacent the stem portion of the T-shaped pedestal.

20. The method of Claim 15, further comprising, prior to the step of filling each of the at least one trenches with at least one dielectric material, removing the spacers.

21. The method of Claim 15, further comprising, prior to the step of filling each of the at least one trenches with at least one dielectric material, thermally oxidizing inner surfaces of the at least one trench so as to form an oxide liner.

22. The method of Claim 15, wherein the gate insulator comprises an oxide of silicon.

23. The method of Claim 15, wherein the gate electrode comprises polysilicon.

24. The method of Claim 15, wherein the source and drain regions are doped with p type ions.

25. The method of Claim 15, wherein the source and drain regions are doped with n type ions.

26. A method of forming an isolated junction comprising:

a) lining vertical sidewalls of a trench formed in a surface of a semiconductor substrate with a spacer material;

b) isotropically etching the trench with an etchant that is more selective for the semiconductor substrate than for the spacer material, to form an undercut portion of the trench;

c) removing the remaining spacer material;

d) oxidizing inner surface of the trench;

e) forming air gaps in the undercut portion of the trench by partially filling trench with insulation material; and

f) implanting impurities into a portion of the semiconductor material that overlies the undercut portion of the trench.